The Product Reliability Test Report of AC9810-32

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About This Document

Purpose

This report is published by Hisilicon to provide insight to our customers regarding the reliability of Hisilicon products.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
AC9810-32	V100

Intended Audience

This document is intended for:

- Reliability test engineers
- Hardware engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazard with a medium level of risk which, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazard with a low level of risk which, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a potentially hazardous situation which, if not avoided, could result in equipment damage, data loss, performance deterioration, or unanticipated results.

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Symbol	Description
	NOTICE is used to address practices not related to personal injury.
NOTE	Supplements the important information in the main text. NOTE is used to address information not related to personal injury, equipment damage, and environment deterioration.

Change History

Changes between document issues are cumulative. The latest document issue contains all changes made in previous issues.

Date	Version	Change Description
2025-07-21	01	This issue is the first official release.

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1 Instruction

This report is published by Hisilicon to provide insight to our customers regarding the reliability of Hisilicon products. Reliability is defined as product performance to specification over time in response to varied environmental stress conditions. The ultimate goal of our reliability program is to achieve continuous improvement in the robustness of the product being evaluated.

As part of this program, finished product reliability is measured periodically to ensure that the product performance meets or exceeds internal and external reliability specifications. Reliability programs are executed in response to internal programs as well as to individual customer requirement. All tests are performed or supervised by experienced Hisilicon employees using facilities that are approved and audited by Hisilicon for compliance to the requirements of JEDEC and MIL-STD-883.

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2 Definition

2.1 Pre-conditioning Test

The Surface Mount Pre-conditioning Test is used to model the surface mount assembly conditions during component solder processing. Consistent with JEDEC JESD22-A113 "Pre-conditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", the devices are subjected to bake for 24 hours, at 125℃ to baseline the package moisture content, a controlled moisture soak for 192 hours, at 30℃/60% R. H., followed by 3 thermal cycles through a reflow simulation temperature profile. This pre-conditioning is consistent with JEDEC Moisture Sensitivity Level 3 thermal package moisture sensitivity and dry-pack storage requirements.

2.2 Temperature Cycling Test

The temperature cycling test is intended to assess the product's ability to withstand temperature changes in a field use situation such as system On/Off temperature changes, night/day, and/or severe storage extremes. The test is used to determine the ability of the component and solder interconnects to withstand thermo-mechanical stresses induced by alternating high and low temperature extremes. The test procedure follows the general guidelines listed in the JEDEC standard JESD22-A104. Electrical testing at the interim and final read points ensures that the units on test continue to meet data sheet specifications.

2.3 Unbiased Highly Accelerated Stress Test

The Unbiased HAST test is performed for the purpose of evaluating the reliability of products in humid environments. It is a highly accelerated test that employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture into the product (into the underfill, substrate, etc.). The test is used to assess the robustness of the product, its mechanical integrity, the adhesion strength between interfaces, and susceptibility to corrosion in the presence of ionic contaminants. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g., galvanic corrosion). The test procedure follows the general guidelines listed in the JEDEC standard JESD22-A118. The typical test parameters used are 96 hours at 130℃/85% Relative Humidity (RH).

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2.4 Highly Accelerated Stress Test

The HAST test is performed for the purpose of evaluating the reliability of products in humid environments. It is a highly accelerated test that employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture into the product (into the underfill, substrate, etc.). The test is used to assess the robustness of the product, its mechanical integrity, the adhesion strength between interfaces, and susceptibility to corrosion in the presence of ionic contaminants. The test procedure follows the general guidelines listed in the JEDEC standard JESD22-A110. The typical test parameters used are 96 hours at 130℃/85% Relative Humidity (RH).

2.5 High Temperature Storage Life Test

HTST is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices such as Kirkendall voiding. During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied. This test may be destructive, depending on time, temperature and packaging (if any).

2.6 High Temperature Operating Life Test

HTOL is used to accelerate failure mechanisms which may be activated through elevated operational temperatures and elevated voltage. All devices receive full and standard production screening prior to receiving HTOL stress. Full Electrical test is performed at each read point to verify that the product meets data sheet parameters. Early Life (EL) is defined as the first 4k hours of field operation. Inherent Life (IL) is defined as 26k hours of field operation in addition to the 4k Early Life field hours. The IL portion of the bath tube curve is constant failure rate indicating the intrinsic product reliability. Extended Life (XL) is defined as 70k hours of field operation. This portion of the stress verifies that any wear out mechanisms have not been initiated.

2.7 ESD: Human Body Model

This method is used to classify components for ESD susceptibility from human handling and to determine the limits of the product in an average production environment when handled by humans. The discharge waveform is intended to approximate the ESD event from a human fingertip to a pin of the component while other pins are at ground potential.

2.8 ESD: Charged Device Model

This method is used to classify packaged semiconductor components for ESD susceptibility and to determine the limits of the product in an average production environment when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface. This method may also be used to evaluate components that are shipped as

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wafers or bare chips. To perform the tests, the components must be assembled into a package similar to that expected in the final application.

2.9 Latch-up Test

Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up. This testing is performed to assure a product does not enter a latch up state when exposed to over/under-voltage conditions on supply pins or over/under-current on signal pins.

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3 Product Reliability

3.1 Pre-conditioning Test: MSL 3

表3-1 Pre-conditioning Test (MSL 3) Condition and Result

Reference Procedure	JESD22-A113D
Test Parameter	SAM Analysis & Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	1. Baking 24 hours at 125℃; 2. Moisture soaking at the temperature and humidity: 30℃,60%RH,192 hours; 3. Reflowing 3x at 260℃.
Pass/Fail Judgment	Pass SAM and functional test (A/R=0/1)
Test Result	1 lot (135ea) pass

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3.2 Temperature Cycling Test

表3-2 Temperature Cycling Test Condition and Result

Reference Procedure	JESD22-A104B
Test Parameter	SAM Analysis & Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	-55℃~ + 125℃ (air to air), 700 cycles
Pass/Fail Judgment	Pass SAM and 700 cycles ATE function test (A/R=0/1)
Test Result	1 lot (45ea) pass

3.3 Unbiased Highly Accelerated Stress Test

表3-3 Unbiased Highly Accelerated Stress Test Condition and Result

Reference Procedure	JESD22-A118A
Test Parameter	Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	130℃/85%RH/33.3Psia/96 hours, Unbiased
Pass/Fail Judgment	Pass uHAST 96 hours ATE function test (A/R=0/1)
Test Result	1 lot (45ea) pass

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3.4 Highly Accelerated Stress Test

表3-4 Highly Accelerated Stress Test Condition and Result

Reference Procedure	JESD22-A110D
Test Parameter	Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	110℃/85%RH/17.7Psia/264 hours, Biased
Pass/Fail Judgment	Pass BHAST 264 hours ATE function test (A/R=0/1)
Test Result	1 lot (45ea) pass

3.5 High Temperature Storage Life Test

表3-5 High Temperature Storage Life Test Condition and Result

Reference Procedure	JESD22-A103D
Test Parameter	Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	150℃, 1000 hours, unbiased
Pass/Fail Judgment	Pass 1000 hours ATE function test (A/R=0/1)
Test Result	1 lot (45ea) pass

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3.6 High Temperature Operating Life Test

表3-6 High Temperature Operating Life Test Condition and Result

Reference Procedure	JESD22-A108B
Test Parameter	Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	Stress temperature (T_j)=+125℃, 1000 hours Dynamic biased; V_{stress}=1.3*V_{core}; 1.2*V_{IO} Read points at 168 hours, 500 hours, 1000 hours
Pass/Fail Judgment	Pass function test (A/R=0/1)
Test Result	2 lots (160ea) pass T1000

3.7 ESD: Human Body Model

表3-7 ESD: Human Body Model Test Condition and Result

Reference Procedure	ANSI/ESDA/JEDEC JS-001-2012
Test Parameter	I-V Curve Shift & Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	Force Voltage from ±1500V Test I-V curve of the test chip
Pass/Fail Judgment	Compliance within 10% V+I envelope around REFERENCE I-V curve (pre-zap); ATE test
Test Result	3 lots (TT/FF/SS) Pass ±1500V

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3.8 ESD: Non-socket CDM

表3-8 ESD: Non-socket CDM Test Condition and Result

Reference Procedure	ANSI/ESDA/JEDEC JS-002-2012
Test Parameter	I-V Curve Shift & Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	Force Voltage from ±500V Test I-V curve of the test chip
Pass/Fail Judgment	Compliance within 10% V+I envelope around REFERENCE I-V curve (pre-zap); ATE test
Test Result	3 lots (TT/FF/SS) Pass ±500V

3.9 Latch-up Test

表3-9 Latch-up Test Condition and Result

Reference Procedure	JESD-78D
Test Parameter	I-V Curve Shift & Function Test
Test Structure	AC9810-32
Vehicle	Package type: TFBGA (15mm*15mm)
Method	Current Trigger: ±50~±100mA, step 50mA Voltage Trigger: 1.5VDD_{max} Ambient Temperature: 25℃ & 85℃
Pass/Fail Judgment	<25mA 10mA+I_{normal} >25mA 1.4*I_{normal} ATE test
Test Result	3 lots (TT/FF/SS) pass Current Trigger Pass 100mA Voltage Trigger Pass 1.5VDD_{max}

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4 Failures in Time

4.1 Calculation Method

Hisilicon calculate FIT rate using JESD85 (Methods for Calculating Failure Rates in Units of FITs) standard. The failure rate is calculated using a Chi-squared distribution to predict a 60% confidence level from the small number of failures and limited sample size of the population tested. The failure rate is as:

$$Failure\ Rate = \frac{X^2 * 10^9}{2 * A_T * A_V * (Stress\ Hours) * (Sample\ Size)}$$

Arrhenius Equation was used in calculating thermal acceleration factors A_T. Acceleration factor is based on the junction temperature under HTOL stressing, T_{Jtest}, the junction temperature under use conditions, T_{Juse}, and the activation energy (E_a).

$$A_T = exp\left[\frac{E_a}{K}\left(\frac{1}{T_{Juse}} - \frac{1}{T_{Jtest}}\right)\right]$$

4.2 FIT Result

表4-1 FIT Result

Reference Procedure	JEP122G
Structure	AC9810-32
Activation Energy	0.7eV reported by foundry
Junction Temperature	Use Conditions: 85°C During Stress: 125°C
Operate Voltage	Use Conditions: 3V During Stress: 3.3V
Pass/Fail Judgment	<50 failures/10^9 hours at 60% CL
Result	Pass

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